Amendments to the Drawings:

The attached sheets of drawings include changes to Figs.20-24. These sheets, which include Figs. 20-24 replace the original sheets including Figs. 20-24.

Attachment: Replacement Sheets
Annotated Sheets Showing Changes

REMARKS/ARGUMENTS

Claims 1-9 are pending. The drawings have been amended to correct minor informalities. No new matter has been introduced.

Claims 1, 2, 4, and 5

Claims 1, 2, 4, and 5 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Fujimoto et al. (US 6,393,519).

Applicants respectfully submit that independent claim 1 is novel and patentable over Fujimoto et al. because, for instance, Fujimoto et al. does not teach or suggest a disk adapter and a disk array connected via a switch, and that a destination drive I/O port to which a frame is to be forwarded is determined, according to the type of a command included in an exchange that is transferred between the disk adapter and one of the disk drives.

The Examiner alleges that the disk I/F unit 112 is a disk adapter, the disk drives 120 form a disk array, the selector unit 124 is a switch, and that Fujimoto et al. at column 6, lines 13-21 discloses that a destination drive I/O port to which a frame is to be forwarded is determined, according to the type of a command included in an exchange that is transferred between the disk adapter and one of the disk drives.

Applicants note, however, that the disk I/F unit 112 is connected between the disk drives 120 and the selector unit 124, so that the disk I/F unit 112 and the disk drives 120 are not connected via the selector unit 124. Instead, the disk IF unit 112 is connected to cache memory units 115-1, 115-2 and shared memory units 116-1, 116-2 via the selector unit 124.

Moreover, the selector unit 124 in Fujimoto et al. selects a port of the cache memory units 115-1, 115-2 and shared memory units 116-1, 116-2, not a port of the disk drives 120. Fujimoto et al. discloses that a selector unit (113 or 123 or 124) has an address/command (ADR/CMD) decoder 203, which includes a port number decoder 221 and a required port decision unit 223 (see Fig. 12; column 5, lines 39-54; and column 6, lines 13-21). The port number being selected is not a port number of the disk drives 120, but a port number of the cache memory units 115-1, 115-2 and shared memory units 116-1, 116-2 (see

column 9, lines 25-30). As stated at column 9, lines 39-40, "the selector unit 113, 123 or 124 is simply called a selector unit." "At Step 506, the selector unit issues an access request (REQ) to the shared memory unit or cache memory unit, and then at Steps 507 and 508 an address (ADR) and a command (CMD) are transferred. At Step 509 a memory module to be accessed is selected in the shared memory unit 114, 116 or cache memory unit 115, and thereafter at Step 510 an access acknowledgement (ACK ON) is returned via the selector unit to the SM or CM access controller 52, 53." See column 9, lines 46-54. The selector unit does not determine a destination drive I/O port to which a frame to be forwarded according to the type of a command included in an exchange that is transferred between the disk adapter and one of the disk drives.

For at least the foregoing reasons, claim 1 and claim 2 depending therefrom are novel and patentable over Fujimoto et al.

Applicants respectfully submit that independent claim 4 is novel and patentable over Fujimoto et al. because, for instance, Fujimoto et al. does not teach or suggest a disk adapter and a disk array connected via a switch, and that a path which a frame passes to be transferred between the switch and one of the disk drives is determined, according to the type of a command included in an exchange between the disk adapter and the one of the disk drives.

As discussed above, the disk I/F unit 112 and the disk drives 120 are not connected via the selector unit 124. Instead, the disk IF unit 112 is connected to cache memory units 115-1, 115-2 and shared memory units 116-1, 116-2 via the selector unit 124. Moreover, the selector unit 124 in Fujimoto et al. selects a path to one of the cache memory units 115-1, 115-2 and shared memory units 116-1, 116-2, not a path to one of the disk drives 120. The selector unit does not determine a path which a frame passes to be transferred between the switch and one of the disk drives forwarded according to the type of a command included in an exchange between the disk adapter and the one of the disk drives.

For at least the foregoing reasons, claim 4 and claim 5 depending therefrom are novel and patentable over Fujimoto et al.

Claims 3 and 7-9

Claims 3 and 7-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujimoto et al. in view of Hashemi et al. (US 5,396,596).

Claim 3 depends from claim 1, and further recites that the exchange for reading data and the exchange for writing data are executed in parallel. The Examiner recognizes that Fujimoto et al. does not show this feature, and cites Hashemi et al. for allegedly providing the missing teaching. Even assuming Hashemi et al. discloses that the exchange for reading data and the exchange for writing data are executed in parallel, Hashemi et al. does not cure the deficiencies of Fujimoto et al. in that it also fails to teach or suggest a disk adapter and a disk array connected via a switch, and that a destination drive I/O port to which a frame is to be forwarded is determined, according to the type of a command included in an exchange that is transferred between the disk adapter and one of the disk drives, as recited in claim 1 from which claim 3 depends. For at least the foregoing reasons, claim 3 is patentable.

Similarly, Hashemi et al. does not cure deficiencies of Fujimoto et al. with regard to claim 7, in that it also fails to teach or suggest a disk adapter and a disk array are connected via a switch, and that a destination drive port to which a frame is to be forwarded is determined, depending on whether the type of a command included in an exchange that is transferred between the disk adapter and one of the disk drives is a data read command or a data write command.

As discussed above, in Fujimoto et al., the disk I/F unit 112 is connected between the disk drives 120 and the selector unit 124, so that the disk I/F unit 112 and the disk drives 120 are not connected via the selector unit 124. Instead, the disk IF unit 112 is connected to cache memory units 115-1, 115-2 and shared memory units 116-1, 116-2 via the selector unit 124. Moreover, the selector unit 124 in Fujimoto et al. selects a port of the cache memory units 115-1, 115-2 and shared memory units 116-1, 116-2, not a port of the disk drives 120. For at least the foregoing reasons, claim 7 is patentable.

Similarly, Hashemi et al. does not cure deficiencies of Fujimoto et al. with regard to claim 9, in that it also fails to teach or suggest a switch connecting a disk controller and a plurality of disk drives, and that a destination drive port to which a frame is to be

forwarded is determined, depending on whether the type of a command included in an exchange that is transferred between the disk adapter and one of the disk drives is a data read command or a data write command. For at least the foregoing reasons, claim 9 is patentable.

Hashemi et al. also does not cure deficiencies of Fujimoto et al. with regard to claim 8, in that it fails to teach or suggest a disk adapter and a disk array are connected via a switch, and that a path which a frame passes between the switch and one of the disk drives is determined, depending on whether the type of a command included in an exchange between the disk adapter and the one of the disk drives is a data read command or a data write command. For at least the foregoing reasons, claim 8 is patentable.

Claim 6

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujimoto et al. in view of Tanaka et al. (US 6,915,380). The Examiner recognizes that Fujimoto et al. does not show that the switch selects one of port to port connection paths between a port to which the disk adapter is connected and ports to which the disk drives constituting the disk array are connected to switch each frame inputted to the switch, according to the destination information within the frame. The Examiner cites Tanaka et al. for allegedly disclosing this feature. Even assuming that Tanaka et al. disclose the missing teaching, it does not cure the deficiencies of Fujimoto et al. in that it also fails to teach or suggest a disk adapter and a disk array connected via a switch, and that the disk adapter determines destination information within a frame to be transferred from the disk adapter to one of the disk drives, according the type of a command included in an exchange between the disk adapter and the one of the disk drives.

For at least the foregoing reasons, claim 6 is patentable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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Attachments
RL:rl
60598653 v1

FIG. 20 (PRIOR ART)

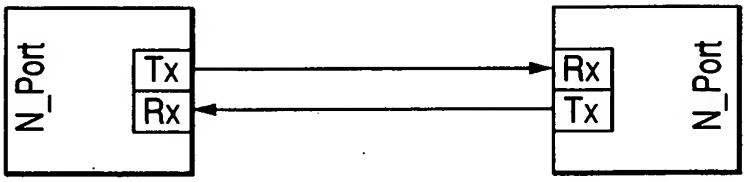

FIG. 21 (PRIOR ART)

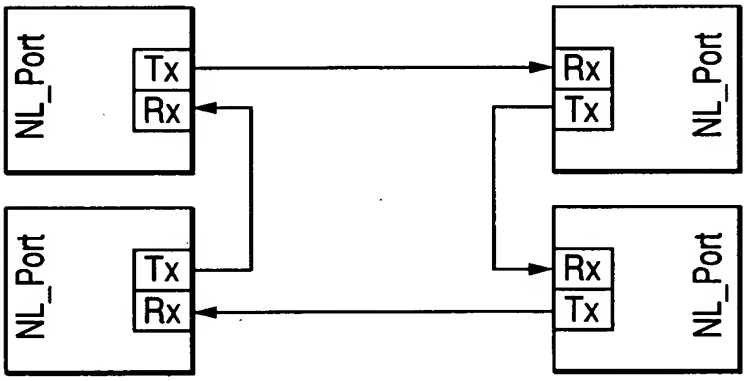

FIG. 22 (PRIOR ART)

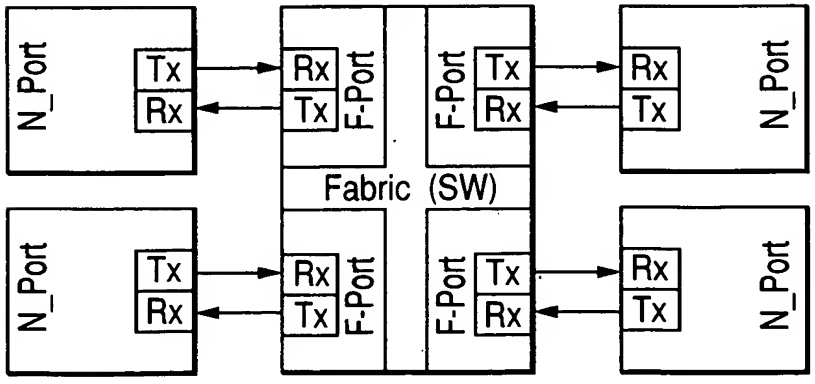

FIG. 23 (PRIOR ART)

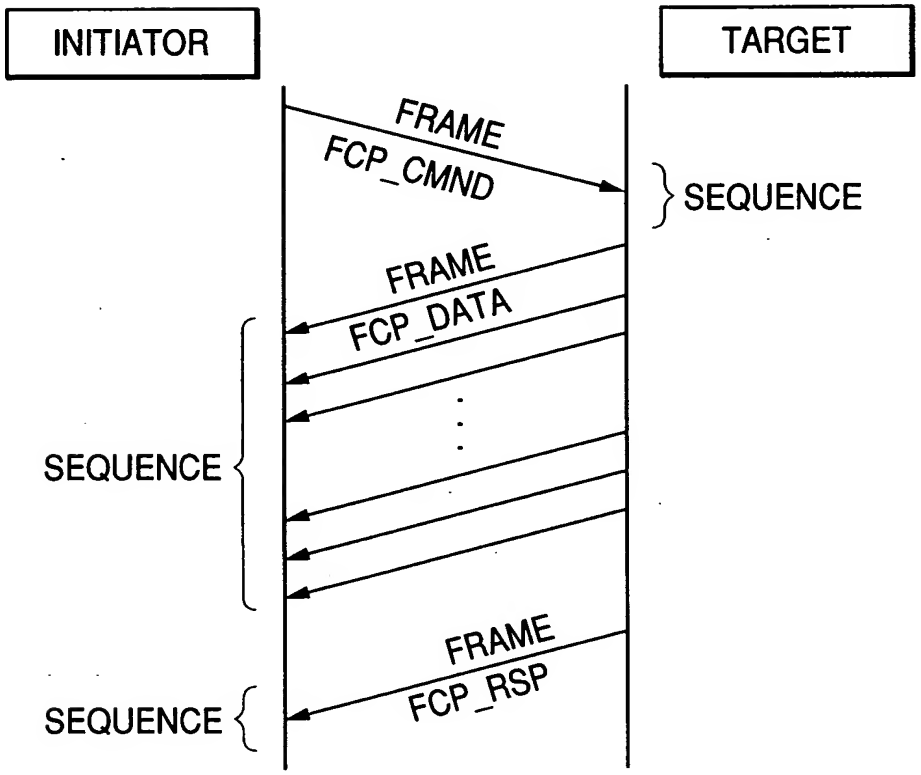

FIG. 24 (PRIOR ART)